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PERFORMANCE ANALYSIS OF A FREQUENCY HOPPING MODEM

A. L. Covitt

DECEMBER 1972

Prepared for

DIRECTORATE OF PLANNING AND TECHNOLOGY

ELECTRONIC SYSTEMS DIVISION
AIR FORCE SYSTEMS COMMAND
UNITED STATES AIR FORCE
L. G. Hanscom Field, Bedford, Massachusetts

Project 511A

Prepared by

THE MITRE CORPORATION
Bedford, Massachusetts

Contract No. F19628-71-C-0002

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FOREWORD

The work described in this report was carried out under the sponsorship of the Directorate of Planning and Technology, Project 511A, by The MITRE Corporation, Bedford, Massachusetts, under Contract No. F19628-71-C-0002.

REVIEW AND APPROVAL

This Technical Report has been reviewed and is approved.

KENNETH H. KRONLUND, Lt Col, USAF
SEEK BUS Program Manager
Development Engineering Division
Directorate of Planning and Technology

ABSTRACT

This report summarizes an analysis of a wide band modem in the presence of Gaussian noise or CW interference. The modem incorporates time division as the multiple access technique, multiple frequency keying as the modulation technique, frequency hopping as the spread spectrum technique and Reed Solomon coding as the error correcting technique. Particular emphasis is placed on synchronization performance using short burst signals.

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SECTION I

INTRODUCTION

Time Division Multiple Access (TDMA) has one important advantage over other multiple access approaches. Since only one transmitter is operating at a time, the suppression of weak signals from distant transmitters by stronger ones from nearby transmitters is avoided. The advantage could be carried still further by using a single waveform and hence a single transceiver to support all communications, navigation, and identification functions. A user with only one transceiver would be able to monitor transmissions from all other users.

Because of the interest in TDMA as a candidate CNI approach, a program was initiated to implement and evaluate various TDMA wideband modems. One of the modem types considered was a frequency-hopping modem designed, fabricated, and tested by Department D-91 of the MITRE Corporation. This modem incorporates time-division as the multiple access technique, multiple frequency shift keying as the modulation technique, frequency hopping as the spread spectrum technique and Reed-Solomon coding as the error correcting technique. This report is intended to provide the theoretical predicted performance for that modem.

Section II contains a brief description of the modem. Sections III, IV and V provide analysis of modem performance. Although the experimental modem was protected against casual interference, no attempt was made to increase the design complexity for

AJ protection. Therefore, the subject of AJ performance is not treated in this report.

SECTION II

THE MODEL FH MODEM

2.0 GENERAL

This section describes a model configuration for a frequency hopping (FH) modem. The model is an idealized version of the experimental hardware which is to be evaluated in laboratory tests.

2.1 Signal Structure

The FH modem employs a pulse transmission structure consisting of a sequence of single frequency rf tone bursts frequency hopped at 20 μsec chip intervals over an RF frequency band of 10 MHz nominal width. Each chip is transmitted at one of 63 burst frequencies separated by intervals of 153.6 KHz. The sixty-three signalling frequencies are subdivided into seven contiguous sub-bands. The lowest frequency in each sub-band is the sub-band carrier and the remaining eight are used to transmit coded octal FSK data.

The message structure is indicated in Table 1.

TABLE 1

MESSAGE STRUCTURE

Word No.	Function	Duration Chips	Bits	μsec	Remarks
1	Coarse Sync Preamble	7	--	140	Carrier hopping pattern
2-3 incl	Fine Sync -- Address	14	12	280	Used to refine timing
4-54 incl	Data	357	306	7140	Fixed length test message
54	TOTALS	378	318	7560	

The coarse sync preamble is the carrier hopping pattern. It is convenient, but not essential, that the pattern chosen be a Reed-Solomon codeword.

The fine sync pattern, consisting of two R/S codewords, also provides a 12 bit address capability. Leading edge measurements made on individual chips of the fine sync word are used to refine receiver timing.

The balance of the message structure contains the capability to transmit 51 six bit source data words.

2.2 General Description of the Model FH Modem

The description of the model FH modem contained in this section has been broken down by function into a format convenient for later analysis. It should be noted that key components of the model appearing in the description of more than one function would not be duplicated in actual implementation. For example, a single synthesizer generates frequencies needed for both transmitting and receiving FH signals. It is characteristic of a TDMA system that only one transmitter is active in a time slot. Therefore, it is possible to disable a modem receiver during the transmit time slot and reuse common components to generate the transmitted signal.

2.2.1 Transmitter

Figure 1 is a simplified block diagram of the model FH modem transmitter. The heart of the modem is a fast acting digitally controlled synthesizer. Digital logic is used to control switching of the synthesizer to generate appropriate chip frequencies at the desired time.

The characteristics of the functional blocks appearing in Figure 1 are:

(1) Timing/Control. All timing for the modem is derived from a 20 MHz frequency standard oscillator synchronized to an outside source. Various timing pulse trains are obtained by digital frequency division and multiplication of subharmonics. A

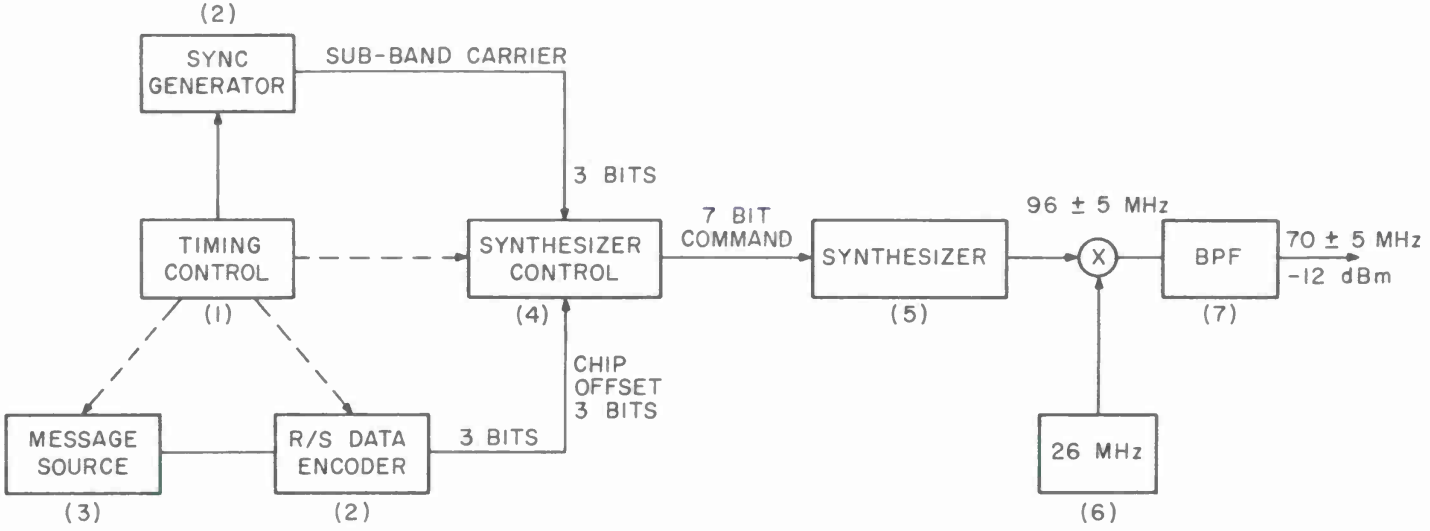

Figure 1 FH MODEM TRANSMITTER

50 KHz pulse train of message length is used to time the sequence of 20 μsec chips delivered from the transmitter.

(2) Sync Generator and B/S Data Encoder. The sync generator and R/S data encoder consist of a twin set of cyclic shift register code generators as illustrated in figure 2. Each of these code generators generates a particular codeword consisting of a sequence of seven octal numbers. The output codeword is determined by the initial settings of two three stage binary shift registers α and β. At the start of the codeword generation sequence, octal input words ($\alpha = \alpha_2\alpha_1\alpha_0$ and $\beta = \beta_2\beta_1\beta_0$) are set into the α and β registers. The first number in the codeword, γ, is formed by modulo-2 addition of the corresponding stages of the shift registers.

$$^{*}\ \gamma = \alpha \oplus \beta = (\alpha_2 \oplus \beta_2)(\alpha_1 \oplus \beta_1)(\alpha_0 \oplus \beta_0)\ .$$

At 20 μsec intervals, (the chip rate), stepping pulses from timing control cause the β register to change. A new octal word $\beta^1 = \beta_2{}^1\beta_1{}^1\beta_0{}^1$ is formed from the previous one.

$$(\beta_2{}^1 = \beta_0 \oplus \beta_1,\ \beta_1{}^1 = \beta_2,\ \beta_0{}^1 = \beta_1)$$

The second number in the codeword, γ^1, is formed by modulo-2 addition of each stage of the α register with the corresponding new values stored in the β register ($\beta_2{}^1\beta_1{}^1\beta_0{}^1$). The process is iterated until the seven number sequence has been generated.

---

* The symbol $\oplus$ denotes modulo-2 addition according to the following rules:

$0 \oplus 0 = 0$ $\qquad$ $0 \oplus 1 = 1$

$1 \oplus 1 = 0$ $\qquad$ $1 \oplus 0 = 1$

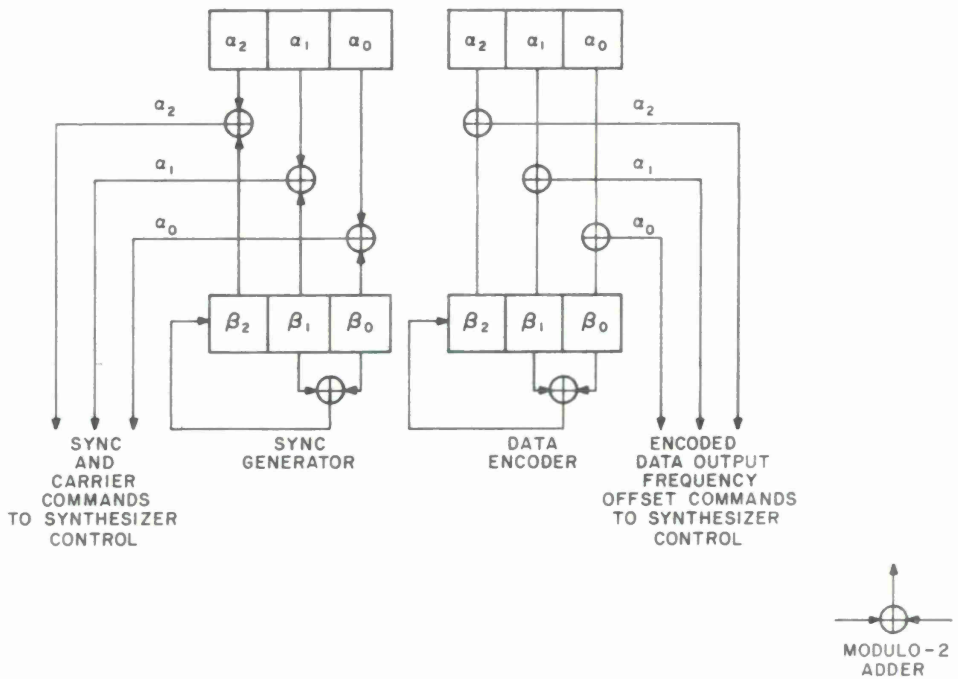

Figure 2 SYNC GENERATOR AND R/S DATA ENCODER

In the experimental modem there is a choice of four preset values for the α, β initializing words in the sync generator. The same seven chip codeword used for the coarse sync preamble is used to control the synthesizer hopping pattern while receiving data.

In the R/S data encoder the α, β initial values represent six data bits read from a message source. After a seven chip codeword has been generated the next six data bits are switched to the α, β registers.

(3) Message Source. The message source is a buffer or preformatted message generator capable of delivering data in six bit increments to the R/S encoder. Each six bit word is read in parallel at the word rate set by timing/control. In the experimental hardware the message source is an 11 stage shift register generator controlled by the same basic timing source as other modem components.

(4) Synthesizer Control. The synthesizer control performs the function of translating octal inputs from the sync generator and R/S data encoder to a two decimal digit frequency command word AB.

The input from the sync generator signifies the particular sub-band desired and the input from the R/S data encoder determines the amount the chip frequency is to be shifted relative to a sub-band carrier. During transmission of the coarse sync preamble, the R/S data encoder output is suppressed, and the chip frequencies called for correspond to the sub-band carriers. During fine sync and data modes, the eight possible values of the R/S data encoder require chip frequencies above the sub-band carrier. The required frequency shifts range from one to nine times the spacing between adjacent frequencies (153.6 KHz).

The decimal frequency command word has 64 possible values $00 \leq AB \leq 63$. The command is transmitted as a seven bit

parallel BCD word. Three bits indicate the seven possible values of the A digit and four bits the ten possible values of the B digit. The command AB directs the synthesizer to switch the outputs of two specific oscillators into a mixer.

(5) Synthesizer. The synthesizer generates frequencies required by both transmitters and receivers from two crystal controlled oscillator banks associated respectively with the A and B digits of the frequency command word. The frequencies of these oscillators are indicated in Table 2.

TABLE 2

SYNTHESIZER OSCILLATOR FREQUENCIES (MHz)

Oscillator No.	A Bank	B Bank
0	39.392	51.6928
1	40.928	51.8464
2	42.464	52.0000
3	44.000	52.1536
4	45.536	52.3072
5	47.072	52.4608
6	48.608	52.6144
7	------	52.7680
8	------	52.9216
9	------	53.0752

The desired A + B product is obtained by mixing one appropriately filtered selection from column a with one from column B.

Through binary-to-decimal converters the frequency command word provides gating signals to a switching matrix. The appropriate A and B signals are switched through isolating amplifiers to a mixer. Filters and a limiting output amplifier help to achieve the following characteristics:

Output level: + 6 dBm

Level variations: approximately 0.25 dB over the band

Settling time: 1 μsec

Harmonics: -35 dB or better

A more complete description of the MITRE synthesizer can be found in MTR-2243 Volume II.

(6) 26 MHz Oscillator. The synthesizer output is contained in a 10 MHz band centered around 96 MHz. The 26 MHz oscillator converts the output to a common 70 MHz IF frequency.

(7) Band Pass Filter. The 10 MHz band pass filter suppresses unwanted out-of-band spurious. The signal is delivered at the filter output at a -12 dBm level.

Translation to rf and amplification to the transmitted power output level is accomplished in an external transceiver.

2.2.2 Coarse Sync Receiver

A simplified functional block diagram of the coarse sync receiver is indicated in figure 3. The essential components of the receiver are:

(1) IF Amplifier. The IF amplifier is an amplifier of nominal 10 MHz bandwidth centered around a 70 MHz IF frequency. In the experimental hardware the amplifier is physically located in the transceiver rather than the modem itself. It is included with the modem functionally to illustrate the essential nature of the interface. The amplifier compensates for losses in the modem and sets the input signal at the desired level. The gain of this amplifier is controlled from the modem after narrowband filtering. The control range is restricted to approximately 30 dB to prevent overload from strong out of band signals.

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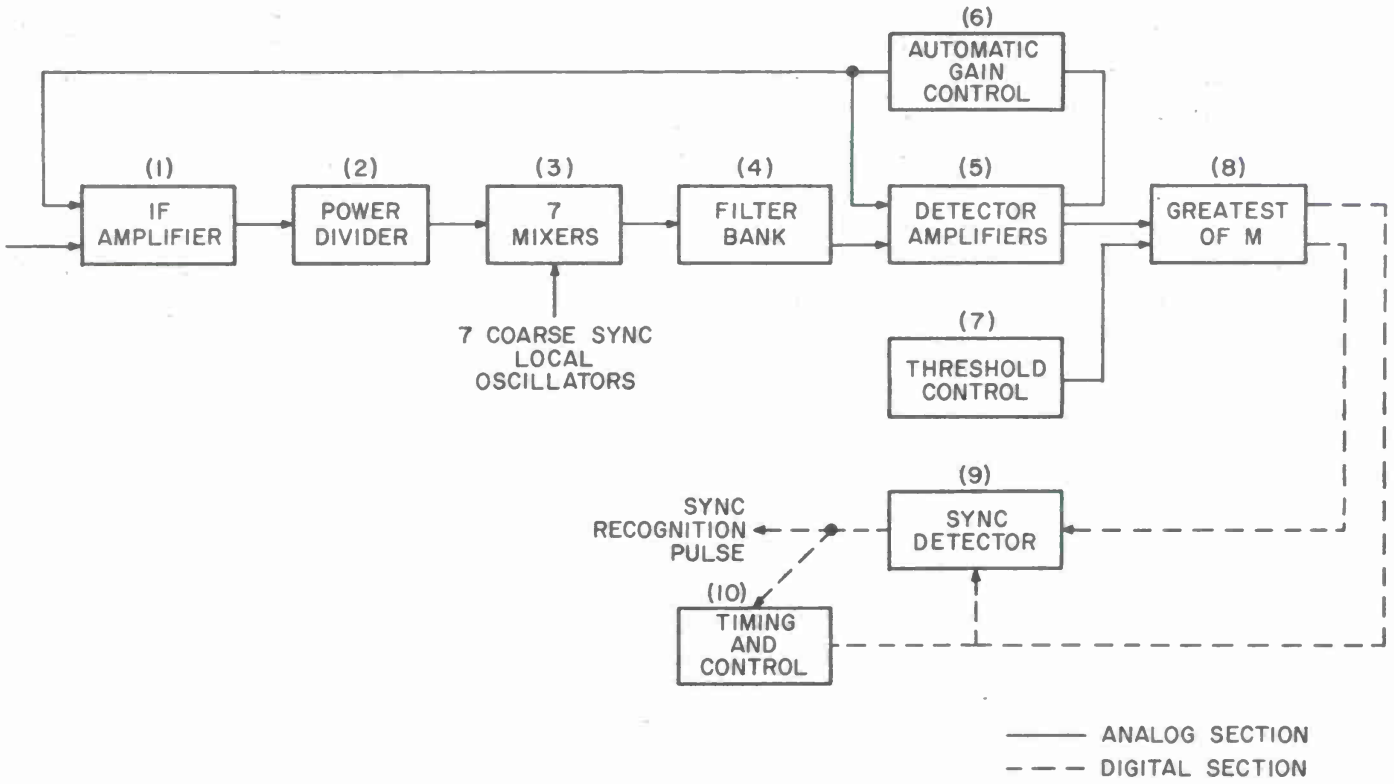

Figure 3 COARSE SYNC RECEIVER

(2) Power Divider. The power divider provides seven parallel transmission paths to be used in the monitoring of the seven different coarse sync frequencies.

(3) Mixers. The mixers convert from the 70 MHz IF frequency to a lower second IF frequency more convenient for filter design. The seven local oscillators used are included as the A bank of crystal oscillators in the synthesizer. (See section 2.2.1 (5)) The outputs of the seven mixers are centered in the respective 100 KHz wide bandpass filters of the filter bank.

(4) Filter Bank. The filter bank consists of seven bandpass 4 pole Butterworth filters each of nominal bandwidth 100 KHz. The center frequencies are:

Filter Number	Midband Frequency MHz
F_0	25.856
F_1	25.692
F_2	25.539
F_3	25.385
F_4	25.238
F_5	25.078
F_6	24.924

(5) Detector-Amplifiers. The detector-amplifiers envelope detect the filter outputs and amplify them to present the appropriate level to the input to the "greatest of" comparison circuit. The gain of these amplifiers is automatically controlled to maintain a nominally constant output level from the filter with the highest output.

(6) Automatic Gain Control (AGC). The AGC consists of a summing amplifier which develops an AGC bias from the sum of the filter envelope voltages. The AGC bias voltage is applied to each

of the detector amplifiers in the modem and to the wideband IF amplifier. Laboratory tests on the experimental modem AGC implemented by B. Mahler showed a $\pm$ 2 dB variation in gain tracking over a 30 dB range of input signals to the detector amplifier. These tests established the feasibility of maintaining within $\pm$1 dB over a 60 dB dynamic range of both:

(a) gain tracking among all channels from the IF amplifier outputs, and

(b) constant level output for the highest filter envelope.

(7) Threshold Control. In order to control the false alarm rate, the output of the greatest of M circuit is inhibited if none of the inputs exceed a threshold value. The threshold control sets a minimum voltage into the greatest of M circuit which must be exceeded if the greatest of eight decision is to be accepted as valid.

(8) Greatest of M Decision Circuit. This circuit compares the inputs and identifies the one with the highest input voltage. The output is a 3 bit digital identification of the specific input which is greatest at any instant of time. The greatest of M circuit has eight inputs. Seven of the inputs in the coarse sync mode are filter envelope voltages. The eighth input channel is used as a threshold. In the coarse sync mode, the circuit determines:

(a) Which of the seven filters has the highest envelope voltage, and

(b) Is that voltage above the threshold?

(9) Sync Detector. The sync detector compares a sequence of seven samples of the greatest of M circuit output accumulated at the chip rate to the expected frequency hopping pattern. If the

comparison indicates 5 or more matches a sync recognition pulse is outputted and receiver dehopping is initiated.

Seven sample sequences are accumulated in sets at 4 times the chip rate to assure that at least one set will be sampled after the filters have had time to respond to the input chip pulse.

The sync detector is provided with a single tone interference rejection circuit. To prevent a strong interfering source from disabling the sync process a counter identifies the number of consecutive samples which indicate identical values for the greatest of M output.

The counter disables the input to the greatest of M circuit from any filter which has the highest envelope for eight consecutive samples (2 complete chip intervals). Assuming that the interference is present before the valid sync signal arrives, the disabled filter will contribute one chip error to the sync recognition process. The detection criterion becomes a match of 5 of the 6 receiving chips. The disabled filter is re-enabled periodically to permit a single sample test for the continued presence of the interference.

(10) Timing and Control. A basic 20 MHz crystal controlled clock with digital multiplier and divider chains is used to control sampling, switching and other digital timing operations within the receiver. Upon receipt of a sync recognition pulse the timing and control circuits switch to a fine sync and data mode.

2.2.3 Fine Sync and Data Receiver

Figure 4 is a simplified functional block diagram of the fine sync and data components used in the model FH modem. Many of the components are identical to those used in the coarse sync receiver

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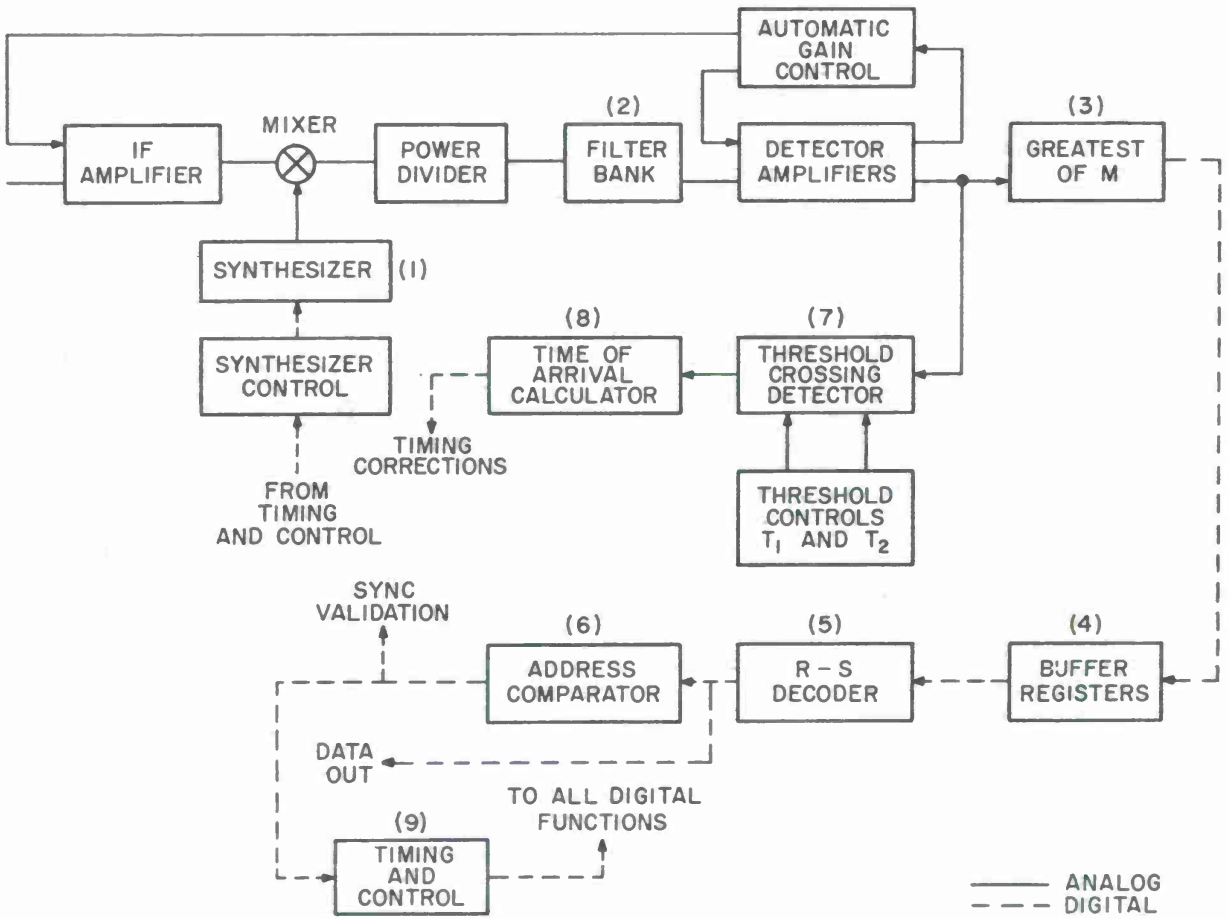

Figure 4 FINE SYNC AND DATA RECEIVER

described in section 2.2.2 and are, in fact, sequentially time shared. The numbered blocks indicate those functions which are either unique to the fine sync and data modes of operation or are modified from the equivalent functions performed in other modes. These modes are:

(1) Synthesizer. In the fine sync mode of operation the synthesizer is used to produce local oscillator signals that will dehop received chips alternately into two filters. One of two filters is used to obtain leading edge measurements of time-of-arrival. Alternate chips are dehopped elsewhere so that the filter used in timing measurements will have sufficient time to settle between samples.

In the data mode the synthesizer uses a dehopping pattern that will input each chip to the narrowband filter signifying the octal (3 bit) data value of the chip.

(2) Filter Bank. In addition to the filters used for coarse sync the model requires an eighth filter, F_7 at a center frequency of 24.771 MHz. This filter is required to permit octal FSK data transmission rather than the 7^{ary} choice used in coarse sync.

In addition to the eighth filter, it was found necessary in the experimental hardware to modify the filter used for leading edge timing measurements. That filter in the experimental modem was a 2 pole Butterworth filter with 175 KHz nominal bandwidth. For the model described in this paper it is assumed that all eight FSK filters are identical in bandwidth and response characteristics. A wider filter, if needed, for time measurements could be provided. In the laboratory, the expediency of space and time considerations dictated that the wider filter be used for both sync and data. The degradation due to non-uniform channel bandwidths was accepted.

(3) Greatest of M. The greatest of M circuit is modified in the model modem to accept an input from filter F_7 instead of the threshold voltage described in section 2.2.2 (8).

For fine sync and data modes M = 8 and the greatest of M circuit identifies the particular one of eight input filters with the highest envelope voltage at sample time.

(4) Buffer Registers. The buffer registers collect and hold seven chip sequences from the greatest of M circuit representing received R/S codewords.

(5) R/S Decoder. The R/S decoder examines each seven chip sequence stored in the buffer register, attempts to identify the transmitted codeword and outputs the six information bits presumed to have been transmitted.

The decoder examines the first two chips (six bits) in each seven chip sequence and uses the encoder described in section 2.2.1 (2) to generate a reference word. The reference word is the 7 octal digit R/S codeword whose first two digits are the six bits examined. From those two octal digits the decoder calculates initial values of α and β for the codeword generator. Each octal number (3 bits) of the reference word is compared with the corresponding octal number of the received sequence. If at least four of the seven comparisons match, the calculated α and β value are outputted as the six bit decoded data word. If there are more than 3 mismatches, the decoder examines the second and third octal numbers in the received sequence and generates a new test word. The process is repeated until:

(a) The codeword matching the 7^{th} and 1^{st} numbers in the sequence fails to match the sequence in at least two additional places. In this case the decoder output is 000000.

(b) The decoder finds a match in at least four positions between the received sequence and the tested word. In this case the six bit output is $\alpha_2\alpha_1\alpha_0\beta_2\beta_1\beta_0$ where α_n is a binary number (1 or 0).

(6) Address Comparator. In the fine sync mode two six bit output words from the decoder are compared with a 12 bit address (fine sync signal). If they do not match exactly the address comparator outputs a pulse indicating that the coarse sync decision has been declared invalid. The receiver then reverts to the coarse sync mode. As will be discussed in section 4.2, beter theoretical performance in the sync mode could be obtained by a direct comparison of the received sequence with the address using a four of seven position match criterion. Bypassing the decoder leaves no possibility of a match with the wrong codeword.

In the data mode, the 6 bit output of the R/S decoder is delivered directly to the data sink.

(7) Threshold Crossing Detector. The threshold crossing detector is used to indicate that the envelope output of a filter has exceeded some threshold voltage. Two threshold comparators are provided to permit the time-of-arrival calculator to compute the slope of leading edge of the filter response.

(8) Time of Arrival Calculation. The time-of-arrival calculator determines the time-of-arrival of fine sync chips relative to dehop timing. The output is a timing offset-calculated in the fine sync mode and applied as a dehop timing correction in the early part of the data mode. The technique used and the variance in measurements is discussed in section 3.3.

(9) Timing and Control. The timing and control function in the data mode includes time-of-day synchronization of the modem clock in addition to the previously discussed functions.

A polling mode operation that transmits time-of-day in both directions between a master and slave modem permits clock offsets to be calculated and corrected. Time-of-day is included in the data transmitted.

SECTION III
SYNC PERFORMANCE IN A GAUSSIAN CHANNEL

3.0 General

The model FH receiver is synchronized in two operational modes. In the first mode, the receiver monitors all frequencies used in the coarse sync preamble. Recognition of the coarse sync signal is a detection decision that initiates dehopping and automatically switches the receiver to the fine sync mode. The fine sync mode refines the dehop timing and validates the coarse sync detection decision.

In the presence of Gaussian noise there are several conditions that can occur which make the sync performance less than perfect. These conditions are discussed briefly in this section and their probabilities of occurrence dealt with in Sections 3.1 to 3.3.

(a) False Synchronization

The possibility exists that a detection decision will be made when no signal is present. The result of this decision is the premature initiation of dehopping in the receiver. The receiver is then incapacitated until restoration of the search mode occurs.

Normally the fine sync mode will find a false sync decision invalid. Because the fine sync message is short the probability that a valid message arrives during the outage period will be low. If a false decision is verified in the fine sync mode, the outage period will correspond to the length of a normal message. During that time, no valid message would be received and a random pseudo-data output would be delivered.

(b) Missed Message

Three types of conditions would produce a failure to receive a valid message:

(1) The receiver may be disabled by a false sync.

(2) Under low signal-to-noise ratio conditions threshold detection criteria may not be met.

(3) A valid detection decision may be falsely invalidated.

(c) Inaccurate Ranging

Time-of-arrival measurements are made on the leading edges of fine sync chips. The dehop timing pulse train is intentionally initiated early with respect to the arrival time of fine sync chips to assure that the receiver is properly tuned to receive the leading edges. This timing error affects fine sync performance in two ways:

(1) Sensitivity of the Sync Validation Process. Early dehop timing cuts off the trailing edge of fine sync pulses and reduces the effective pulse width applied to the narrowband filter. Shortening of the pulses degrades the signal-to-noise ratio at the filter outputs. If the filters are matched to the normal pulse width, the output will not rise to peak signal amplitude in response to the narrow pulse. Alternatively, if the filters are widened to reduce the rise time more noise will be accepted.

(2) Accuracy of Timing Computations. Measurements of threshold crossing time on the leading edges of fine sync chips are used to compute a dehop timing correction. One of the sources of error in this computation is the variance of threshold crossing times due to noise. Shortening the effective pulse width applied to the filters increases this variance.

The accuracy of the timing measurements is most critical if the data is to be used for ranging. A 1 nanosecond error in time corresponds to a 1 ft. error in range.

3.1 Probability of False Synchronization

Pertinent parameters of the model FH coarse sync receiver are:

L = Length of the coarse sync pulse expressed in number of chips used.

M = Number of frequencies monitored by the coarse sync receiver.

{S} = A possible course sync sequence expressed as L numbers taken from the alphabet 1, 2...M. This sequence occurs in the following manner: A greatest of M circuit identifies the particular one of M channel filters with the greatest output at any instant of time. The output of this circuit is sampled at some multiple of the chip rate. A sample set is a particular group of L samples composed of any individual sample and L-1 subsequent samples taken at the chip rate.

K = A detection decision criterion. The coarse sync pulse is represented as L digits. Each digit is compared with the corresponding digit of the {S} sequence. K or more matches are required in the L comparisons.

T = A voltage threshold set on the inputs to the greatest of M circuit to inhibit signals which do not exceed T. This is done to reduce the probability of false synchronizing on noise alone.

A = Mean amplitude of a signal at the input to the greatest of M circuit.

N_o = Noise power density in watts/cycle at the input to the greatest of M circuit.

W = Bandwidth of a narrowband channel filter.

σ = Standard deviation of noise voltage at input to greatest of M circuit

$$\sigma^2 = N_o W$$

p = Probability that a particular digit in a sample set {S} matches the corresponding digit in the coarse sync code.

P_F = Probability of a false detection decision.

When no signal is present and the input to the receiver is Gaussian noise, the inputs to the greatest of M circuit are statistically identical Rayleigh distributed noise voltages.

For this condition,

$$p = \int_T^\infty \frac{x}{\sigma^2} \, e^{-\left\{\frac{x^2}{2\sigma^2}\right\}} \left[\int_0^x \frac{y}{\sigma^2} \, e^{-\frac{y^2}{2\sigma^2}} \, dy \right]^{M-1} dx \qquad (1)$$

x and y are dummy variables in equation (1). Equation (1) reduces to

$$p = \sum_{i=0}^{M-1} \frac{(-1)^i}{i+1} \binom{M-1}{i} e^{-\frac{(i+1)T^2}{2\sigma^2}} \qquad (2)$$

The probability of a false coarse sync detection decision is given by:

$$P_F = \sum_{i=K}^{L} \binom{L}{i} p^i (1-p)^{L-i} \qquad (3)$$

Equation (3) represents a coarse sync detection criterion of K or more matches in a sample set {S} consisting of L numbers

Equations (2) and (3) have been evaluated at a few points for K=5, L=7, M=7 the values used in the coarse sync mode of the model modem. Results are tabulated below:

Threshold T	p	P_F
0*	.14286	9.78×10^{-4}
σ	.14265	9.54×10^{-4}
2σ	.09111	1.127×10^{-4}
3σ	1.074×10^{-2}	2.94×10^{-9}
4σ	3.4×10^{-4}	9.54×10^{-17}

3.2 Probability of Missed Messages

There are three reasons why a message transmitted in a particular time slot may not be received. Factors contributing to the probability of a missed message in the model FH modem are:

(1) The probability that the receiver is disabled by a false synchronization decision when the desired signal arrives,

(2) The probability that coarse sync detection criteria are not met at the time a valid signal is present at the receiver,

(3) The probability of non-recognition of the fine sync signal after a valid coarse sync detection has been made.

These three probabilities are considered in sections 3.2.1 to 3.2.3.

3.2.1 Probability of Disabled Receiver Causing a Missed Message

In the operating TDMA environment it is assumed that:

(a) Modem clocks are synchronized to a common system time,

(b) A transmission occurs at the beginning of each time slot.

(c) Guard times of 2 to 3 ms are provided to allow for maximum line-of-sight transmission range of approximately 400 to 600 miles and a modest timing error such that no valid message is received outside of an assigned time slot.

* This corresponds to omitting the threshold circuit.

(d) Model FH modems are in the coarse sync acquisition mode at the beginning of each time slot.

(e) Users are randomly distributed in range with an average range corresponding to approximately 1 ms delay.

Under the above assumptions, it is only necessary to consider the effect of false coarse sync detection decisions that occur in the interval between the beginning of a time slot and the arrival of a valid message.

The probability that a false coarse sync decision occurs in the interval between the beginning of a time slot and the message arrival time is approximately the product of:

(1) P_F, the probability that a false alarm occurs in one sample set {S}, and

(2) The number of independent sample sets.

Although sample sets are accumulated at many times the chip rate, filter bandwidths limit the maximum rate of change of the noise envelopes. The model modem uses 100 KHz band pass filters at IF. These filters are equivalent to 50 KHz at baseband. The effective rate of accumulation of independent samples for this bandwidth is assumed to be 1 sample per 10 μ seconds.

If the receiver makes a false coarse decision it will be incapacitated for at least 280 μsec (the time required to accumulate sufficient data to test the validity of the decision.)

The effect of this false alarm is contingent upon the outcome of the fine sync validation test discussed in sections 3.2.1.1 and 3.2.1.2.

3.2.1.1 Case I. The coarse sync decision is found invalid. A valid message will be missed if the false dehopping mode started at any time during the 280 μsec interval immediately preceding the

arrival of the valid message. Since there are 28 independent samples during this interval the probability of a missed message is

$$P_M = 28 \times 9.78 \times 10^{-4} = 2.74 \times 10^{-2}$$

Although a false alarm threshold can reduce this probability to a negligible value a threshold setting may be undesirable under marginal signal-to-noise or strong interference conditions.

3.2.1.2 Case II. The false coarse sync decision is validated. In a false dehopping mode the receiver may mistake 14 samples of the greatest of M circuit output for the fine sync signal. In this condition the receiver cannot accept a valid message and will output false data for the duration of the apparent message.

The probability of false validation depends on the decoding algorithm used as indicated in the following examples:

(a) Maximum Likelihood Decoder

A maximum likelihood decoder compares a 7 number sequence from the greatest of M circuit with each of 64 codewords. The decoder selects the codeword matching in the greatest number of places. If there is no single codeword agreeing in more places than all others, the decoder will make an equal probability selection of one codeword from the closest alternatives. This decoder has the maximum error correcting capability. However, it does not have the lowest possible false alarm rate. When the input is random noise the probability that any specific codeword is selected is 1/64. The probability of false validation is $1/64^2 = 2^{-12} = 2.44 \times 10^{-4}$.

(b) Threshold Decoder

A very simple decoding technique consists of comparison of a seven number input sequence with a seven number reference word.

If the two agree in four or more places, the decoder accepts the reference word. If this threshold is not exceeded the input is simply rejected as uncorrectable. In the fine sync mode the receiver uses the 14 chip fine sync address as two consecutive reference words. Fine sync validation occurs when both reference words meed the 4 of 7 acceptance criterion. The probability of sync validation Pv for this decoder is:

$$Pv = \left[\sum_{i=4}^{7} \binom{7}{i} p^{i}(1-p)^{7-i} \right]^{2} \qquad (4)$$

When the input to the receiver is noise only, the probability, p, of a single chip match is 1/8 and Pv is the probability of false sync validation. For this situation $Pv = 3.89 \times 10^{-5}$.

(c) Sequential threshold Decoder

The experimental hardware uses a decoding algorithm suggested by C. Wolverton. Any pair of numbers in a sequence of seven octal numbers is contained in one R/S codeword. The decoder generates as a reference word the R/S codeword that matches the first two numbers in the input sequence. If two or more additional matches are found between the reference and the input sequence the decoder accepts the reference. If the threshold criterion is not satisfied, the test is repeated with the codeword containing the second and third numbers of the input sequence. The process is repeated until:

(1) A match in four or more places is found, or

(2) The seventh trial using the codeword containing the first and last numbers in the input sequence fails.

This decoder has a slightly lower false validation probability than the simple threshold decoder discussed in example (b).

The probability that the decoder in example (b) will accept a sequence that matches the fine sync signal in exactly 4 of 7 places is:

$$\binom{7}{4} p^4(1-p)^3 = 35\, p^4(1-p)^3$$

However, 8% of the sequences that match one codeword in exactly four places will also match a second codeword in four places. The sequential decoder will choose between alternatives with equal probability. The probability that the sequential decoder will generate the fine sync sequence as a reference when it agrees in exactly four of seven places with the random input sequence is:

$$96\% \text{ of } 35\, p^4(1-p)^3$$

Hence, the probability of validation for the sequential decoder is

$$Pv = \left[33.6\, p^4(1-p)^3 + \sum_{i=5}^{7} \binom{7}{i} p^i(1-p)^{7-i}\right]^2 \qquad (5)$$

From the assumption that the average signal arrives 1 ms after the beginning of the time slot, there are 100 independent sample sets {S} collected. The probability that a false coarse sync decision occurs and is validated is $100\, P_F P_v$. For the threshold decoder this probability is 3.8×10^{-6}.

3.2.2 Probability of Failure to Cross the Detection Threshold

The criterion for a sync decision is a match of K or more of L digits in a sample set with the corresponding digits of the sync code. This criterion is expressed in equation (3). In that

equation, the digit matches were due to noise alone and a detection decision represented a false alarm. When a valid coarse sync signal is present the same equation is used to compute the probability of detection. Let P_r be the probability of rejecting a valid signal.

$$P_r = 1 - \sum_{i=K}^{L} \binom{L}{i} p_S^{\,i} (1-p_S)^{L-i} \qquad (6)$$

where p_S corresponds to the probability of a chip match when signal is present.

Several simplifying assumptions are made in formulating an expression for p_S when signal is present. It is assumed that signal is present only in one filter at a time, that is, crosstalk, intersymbol interference, variations in sensitivity with frequency and similar sources of performance degradation are neglected.

When signal is present, the inputs to the greatest of M decision circuit will have two different probability distributions. The channel containing signal will have a Rician probability distribution and the others will be Rayleigh distributed. With signal present, equation (1) is modified to:

$$p_S = \int_T^{\infty} \frac{x}{\sigma^2} e^{-\frac{(x^2+A^2)}{2\sigma^2}} I_0\left(\frac{xA}{\sigma}\right) \left[\int_0^x \frac{y}{\sigma^2} e^{-\frac{y^2}{2\sigma^2}} dy \right]^{M-1} dx \qquad (7)$$

Equation (7) reduces to equation (1) when A = 0.

Schwartz, Bennett and Stein* evaluate an integral similar to (7) to obtain the probability of an error in an incoherent binary FSK system. They solve for the special case where T=0 and M=2.

* Communications Systems and Techniques - McGraw-Hill, 1966.

The second integral in equation (7) is straightforward and becomes:

$$1 - e^{-\frac{x^2}{2\sigma^2}}.$$

In the general case, expansion of

$$\left(1 - e^{-\frac{x^2}{2\sigma^2}}\right)^{M-1}$$

produces a series of terms of the form ae^{-bx^2}. The similarity of these terms to the integral evaluated by Schwartz, et al. permits an extension to the m'ary case.

$$1 - p_S = \sum_{n=1}^{M-1} \frac{(-1)^{n+1}}{n+1} \binom{M-1}{n} e^{-\frac{nA^2}{2(n+1)\sigma^2}} \tag{8}$$

When the model FH modem is in the coarse sync mode, the constants (K, L, M) of equations (6) and (8) are (5, 7, 7). The probability that the "greatest of" circuit makes an incorrect digit decision, when signal is present, is shown as a function of SNR in figure 5. A valid coarse sequence is rejected if the sequence {S} does not agree in 5, 6, or 7 digit positions with the stored sequence. The probability of rejecting a valid sync sequence is shown as a function of SNR in figure 6.

The mean signal amplitude, A, (and consequently the chip signal-to-noise ratio $A^2/2\sigma^2$) depends on sample timing and filter response. In the modem implemented in the laboratory, coarse sync sets {S} are accumulated at four times the chip rate to assure that

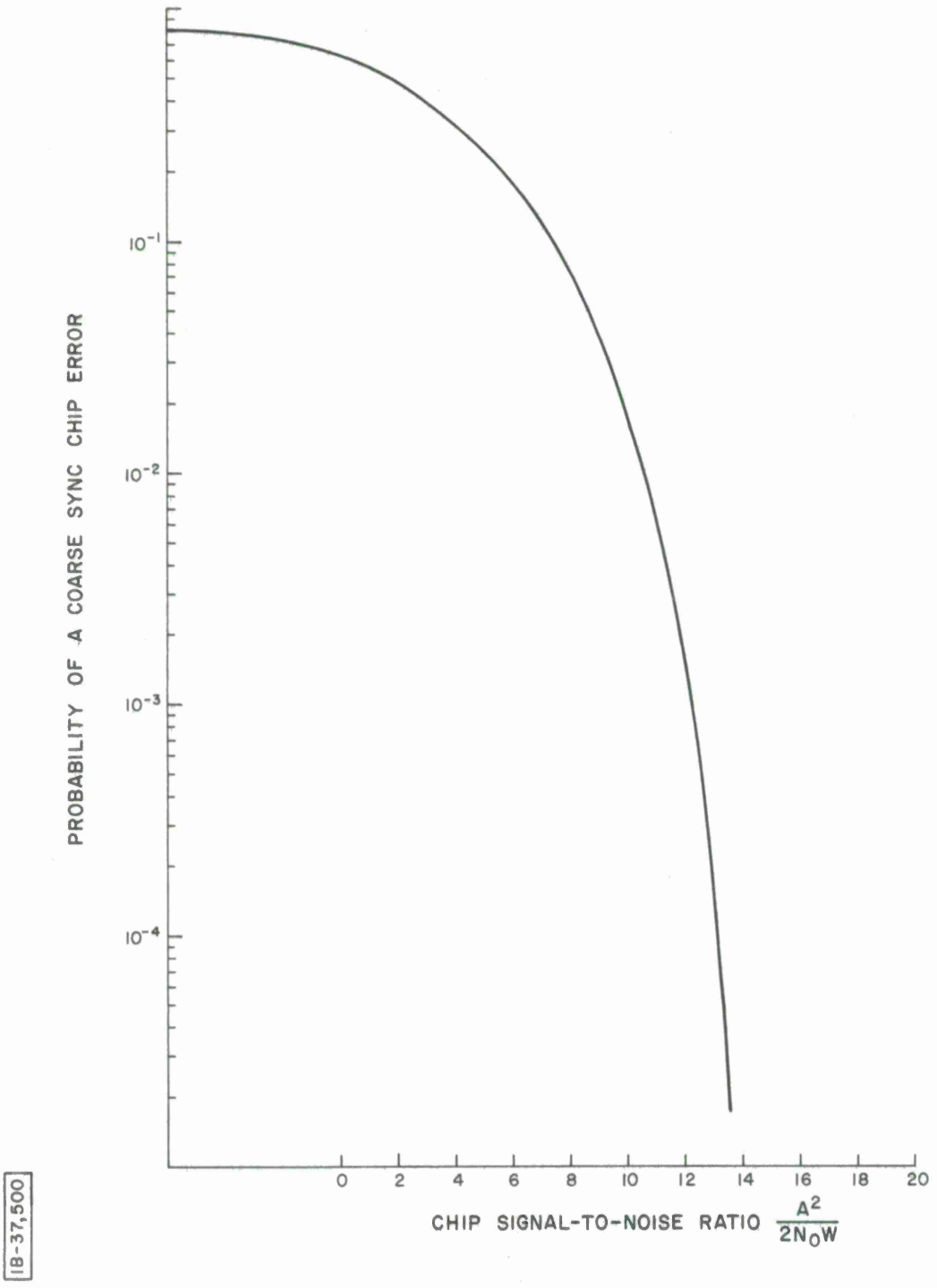

Figure 5 PROBABILITY OF A COARSE SYNC CHIP ERROR IN A GAUSSIAN CHANNEL

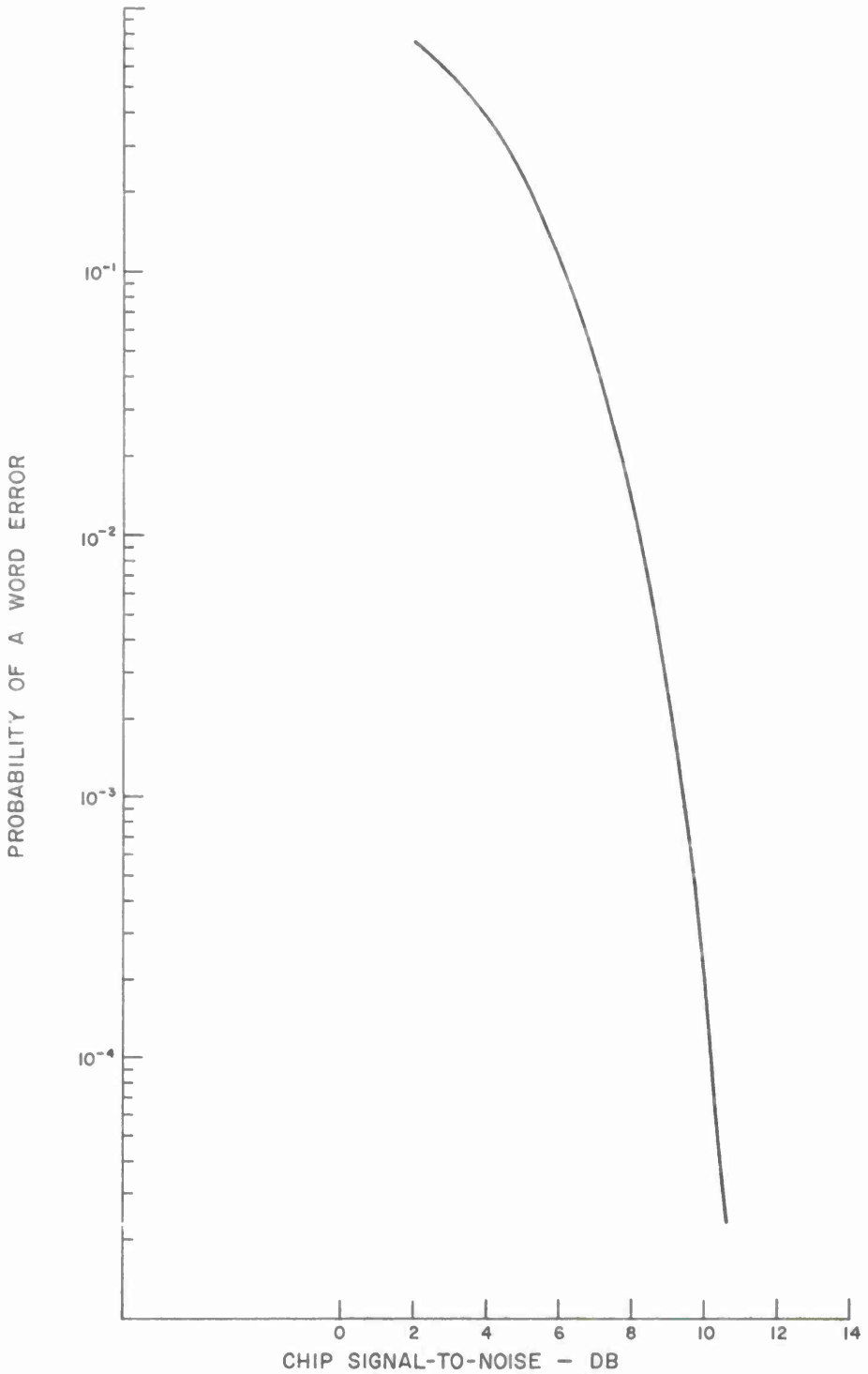

Figure 6 PROBABILITY THAT A VALID COARSE SYNC SIGNAL IS MISSED IN A GAUSSIAN CHANNEL

at least one sample will occur near the peak of a filter response. A coarse sync detection failure requires rejection of all four sample sets. However, it is very unlikely that a failure to detect coarse sync in the most favorably timed sample would be immediately preceded by a successful detection at a lower signal-to-noise ratio. Hence, probability of missing a valid sync per time slot is also given by the curve in figure 6.

3.2.3 Probability of Fine Sync Failure

The process of address recognition in the modem receiver is used to validate the coarse sync detection decision. The two R/S codewords received immediately after the coarse sync pulse are compared digit-for-digit with the expected address. A match of at least four of seven digits in each of the two words is the criterion used for validation.

The probability of invalidating a valid coarse sync, P_I, is given by:

$$P_I = 1 - (1-P_r)^2 \qquad (9)$$

when P_r is the probability of rejecting a valid R/S (obtained from equation (6)). Constants used in equations (6) and (8) to calculate chip and word error rates are (K, L, M) = (4, 7, 8). Results of these calculations are plotted in figure 7.

3.3 Accuracy of Fine Sync Time of Arrival Measurements

In the fine sync mode, a chip consisting of a single frequency tone burst with a nominally rectangular envelope is passed through an IF bandpass filter. The pulse envelope of the filter output is used for time of arrival measurements. Time-of-arrival is

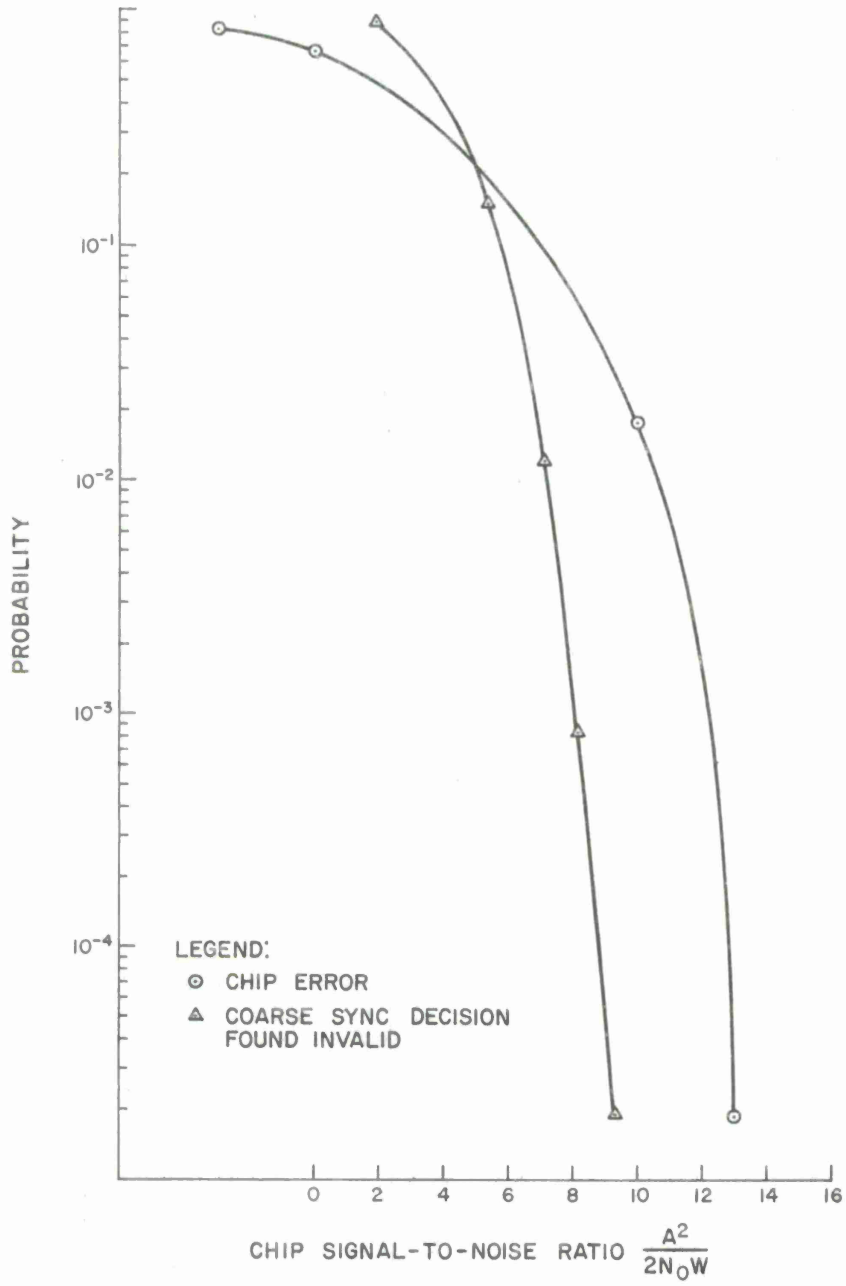

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Figure 7 PROBABILITY OF FINE SYNC FAILURE IN A GAUSSIAN CHANNEL

computed from measurements made of leading edge threshold crossing times and known filter response characteristics.

Figure 8 presents a linearized approximation of the leading edge response of a filter to a step function. It is assumed that the chip duration is long compared to filter rise times and delays such that the full amplitude A is reached before the end of the chip.

Several reference times are indicated in figure 8:

(1) $t = 0$, the time origin is taken as the instant when the receiver is tuned to accept the fine sync chip sequence. This time is determined in the coarse sync mode.

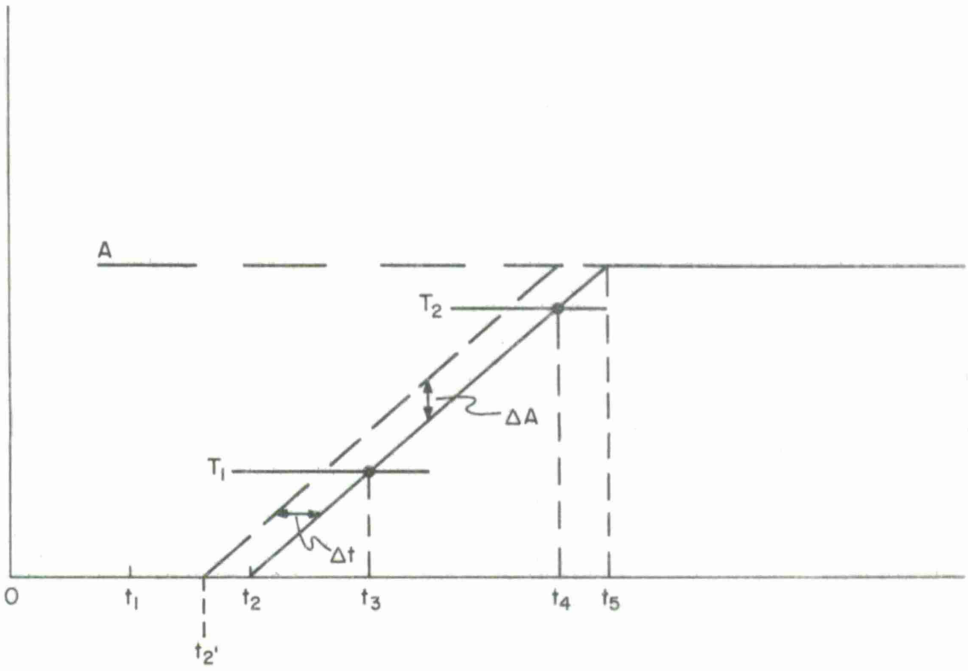
(2) t_1, is the time the chip arrives at the filter input. This is the dehop timing offset.

(3) t_2, is the time the filter output begins to rise. A precursor delay $t_p=t_2-t_1$ is characteristic of the specific filter used.

(4) t_5 is the time the linearized leading edge reaches full amplitude A. The rise time for this idealized filter is defined as $t_r=t_5-t_2$. In a practical filter design the leading edge is reasonably linear between 20% and 80% of full amplitude. The linearized leading edge approximation is the line drawn through these points.

(5) t_3 and t_4 are the times that arbitrary thresholds T_1 and T_2 are crossed by the leading edge of the output envelope.

In the absence of noise or signal level variation any arbitrary point on the leading edge may be used for a time measurement. For example the time t_3 when threshold T_1 is crossed and the known slope of the leading edge, A/t_r, may be used to compute the intercept t_2. When the precursor t_p is subtracted, t_1 is established. t_1 is the dehop timing error to be removed after completion of the fine sync.



t_1 = TIME RECTANGULAR PULSE APPLIED TO FILTER

t_2 = TIME FILTER OUTPUT BEGINS TO RESPOND

t_3 = TIME OUTPUT CROSSES THRESHOLD T_1

t_4 = TIME OUTPUT CROSSES THRESHOLD T_2

t_5 = TIME OUTPUT REACHES AMPLITUDE A

$t_2 - t_1 = t_p$ = PRECURSOR DELAY

$t_5 - t_2 = t_r$ = FILTER RISE TIME

ΔA = VARIATION IN ENVELOPE AMPLITUDE DUE TO NOISE

$\Delta t = t_{2'} - t_2$ = ERROR IN ESTIMATING t_2

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Figure 8 IDEALIZED LEADING EDGE FILTER RESPONSE

Three sources of error in the estimation of t_1 are amplitude variations, noise and clock quantization. The effects of these errors are discussed in sections 3.3.1 to 3.3.3.

3.3.1 Errors Due to Amplitude Variation

From the geometry of figure 8;

$$\frac{A}{t_r} = \frac{T_1}{t_3 - t_2}$$

Therefore,

$$t_2 = t_3 - \frac{t_r T_1}{A} \tag{10}$$

If the amplitude, A, and filter rise times were known no other threshold crossing measurement would be needed. The sensitivity of a single threshold crossing measurement to amplitude variations is obtained by differentiating equation (10)

$$dt_2 = t_r \cdot \frac{T_1}{A} \cdot \frac{dA}{A} \tag{11}$$

For t_r = 5 μsec and T_1 set at 40% nominal amplitude

$$dt_2 = 2 \frac{dA}{A} \text{ μsecs}$$

If the amplitude can be held constant to ± 1 dB (e.g., by an accurate AGC) the maximum chip to chip amplitude variation will be of the order of $\pm 12\%$. The corresponding peak error in the timing measurement is ± 240 nanoseconds. The rms error in a single measurement will be less than the peak value. A further reduction in the rms error by a factor of 7 will occur when independent measurements are averaged over seven fine sync chips.

Amplitude sensitivity can be reduced by adding a second threshold T_2 to facilitate measurement of the leading edge slope. From figure 8

$$\frac{A}{t_r} = \frac{T_2 - T_1}{t_4 - t_3} \tag{12}$$

Substitution of equation (12) in equation (10) yields the result:

$$t_2 = \frac{t_3 T_2 - t_4 T_1}{T_2 - T_1} \tag{13}$$

Although A has been eliminated from equation (13), the two threshold technique is not, in practice, amplitude insensitive. For a 4 pole Butterworth filter the constant slope leading edge approximation to the step function response is not completely valid. The slope is reasonably constant from 20% to 80% of full amplitude. With the two thresholds set at nominal values of 30% and 60% of the mean amplitude, the linear dynamic range is about 6 dB. Linear dynamic range is defined here as the ratio of (a) the maximum amplitude for which

$$\frac{T_1}{A} > .2$$

to (b) the minimum amplitude for which

$$\frac{T_2}{A} < .8$$

Although the two threshold approach suggested by P. Bratt and Dr. Myron Leiter does permit some relaxation in the requirement for uniformity of amplitude with chip frequency, the technique introduces some problems not encountered in the single threshold implementation. For example, under certain multipath conditions, the leading edge of the filter output pulse is badly distorted. The lowest usable threshold setting of T_1 might permit a reasonable single threshold estimate of time-of-arrival to be made on the earliest arriving signal components. In the two threshold approach disturbing multipath components may arrive in the interval between threshold crossings.

3.3.2 Errors Due to Noise

The dehop timing offset t_1 of figure 8 is determined by subtracting the precursor, t_p, from the average of seven estimates of t_2. Equation (13) describes the nominal relationship between t_2 and crossings of two thresholds T_1 and T_2.

When the effects of noise are taken into account, a single estimate of t_2 is given by:

$$\hat{t}_2 \equiv t_2 + E_2 = \frac{T_2}{T_2-T_1}(t_3+E_3) - \frac{T_1}{T_2-T_1}(t_4+E_4) \qquad (13a)$$

where E_n denotes an error in the definition of t_n.

The variance of the single estimate is:

$$\overline{E_2^2} = \frac{T_2^2}{(T_2-T_1)^2}\overline{E_3^2} + \frac{T_1^2}{(T_2-T_1)^2}\overline{E_4^2} - \frac{2T_1T_2}{(T_2-T_1)^2}\overline{E_3E_4} \qquad (14)$$

Skolnik* derives an approximation for the noise produced jitter in the leading edge of a pulse. The essence of the approximation, valid for high signal-to-noise ratios, is that a small perturbation in pulse amplitude does not alter the slope of the leading edge. Stated another way, the variance in the time of a threshold crossing is assumed independent of the level at which the threshold is set. Under conditions where the Skolnik approximation is valid $E_3^2 = E_4^2$ and equation (14) reduces to:

$$\overline{E_2^2} = \frac{\overline{E^2}}{(T_2-T_1)^2}[T_2^2 + T_1^2 - 2\rho T_1T_2] \qquad (14a)$$

where $\overline{E_3^2} = \overline{E_4^2} \equiv \overline{E^2}$ and $\rho \equiv \overline{E_3E_4}$ is the correlation coefficient between the jitter in the measurements of t_3 and t_4. Under various conditions ρ can vary over the range $1 \geq \rho \geq -1$.

* Skolnik, Introduction to Radar Systems - McGraw-Hill, 1962, p. 464.

The value of ρ for white noise into a filter having a constant slope response to a step function can be shown to be

$$\rho = 1 - \frac{t_4 - t_3}{t_r} = 1 - \frac{T_2 - T_1}{A} \tag{15}$$

Skolnik's result for the relationship between amplitude perturbations and timing jitter is readily obtained from the geometry of figure 8.

$$\frac{\Delta t}{t_r} = \frac{\Delta A}{A}$$

$$\frac{\overline{E^2}}{t_r^2} = \frac{\overline{\Delta A^2}}{A^2} = \frac{1}{2} \cdot \frac{2N_o W}{A^2} \tag{16}$$

Figure 9 is a plot of the rms error in the timing offset measurement normalized to the filter rise time. The Skolnik approximation for a single threshold crossing, curve #(1), is obtained from equation (16) by defining a variance: $\sigma_1^2 \equiv \overline{E^2}$

$$\frac{\sigma_1}{t_r} = (2\ \mathrm{SNR})^{-1}$$

where SNR is the signal-to-noise ratio.

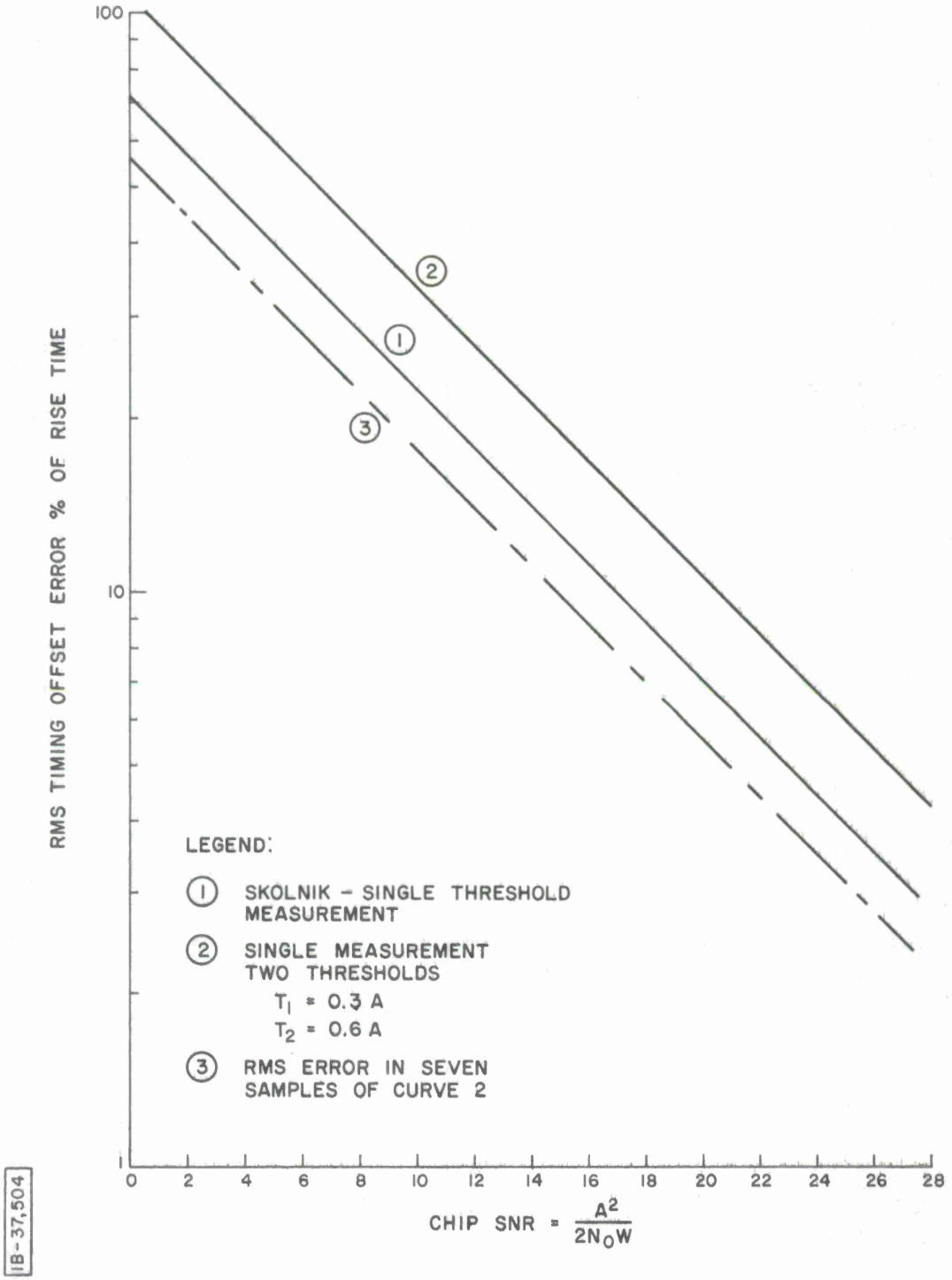

Figure 9 RMS ERROR IN TIMING OFFSET NORMALIZED TO PERCENTAGE OF RISE TIME

Curve #(2) is obtained from equations (14a) and (15) for the double threshold crossing case with a variance: $\sigma_2^2 \equiv E_2^2$

$$\frac{\sigma_2}{t_r} = k \frac{\sigma_1}{t_r}$$

The constant, k, is calculated from equation (14a) and (15). Curve #(3) is the rms error in the average of seven estimates of timing offset. Each estimate is based on a two threshold measurement. Curve (3) is very simply:

$$\frac{\sigma_3}{t_r} = \frac{1}{\sqrt{7}} \cdot \frac{\sigma_2}{t_r}$$

3.3.3 Clock Quantization Errors

In the experimental modem the ratio of the thresholds T_2/T_1 is 2. Hence, from (13), the following scheme using a single counter can be employed to estimate t_2:

(1) Zeroing the counter at t = 0

(2) incrementing the counter until threshold T_1 is crossed, and

(3) decrementing the counter until threshold T_3 is crossed.

This estimate is:

$$\hat{t}_2 = \hat{t}_3 - (\hat{t}_4 - \hat{t}_3) = 2\hat{t}_3 - \hat{t}_4 \qquad (13b)$$

We define the quantization error to be

$$q_n \equiv \hat{t}_n - t_n$$

The timing offset due to quantization error, q_2, is

$$q_2 = 2q_3 - q_4 \qquad (13c)$$

Hence

$$\overline{q_2^2} = 4\overline{q_3^2} + \overline{q_4^2} - 4\overline{q_3 q_4}$$

Assuming q_3 and q_4 are independent and each has a uniform distribution between 0 and Δ, where Δ is the interval between clock pulses, then (after a simple computation), the rms quantization error is given by

$$q_2 \text{rms} = \Delta \sqrt{2/3}$$

The effect of clock quantization is to set a floor on the minimum rms error in timing measurements. The curves of figure 9 modified for 100 nanosecond quantization will asymptotically approach minimum rms values of:

(1) Single threshold (Curve 1)

$$\frac{\sigma_{t_{min}}}{t_r} = \frac{1}{5\text{x}10^{-6}} \cdot \frac{100}{\sqrt{3}} \text{ x } 10^{-9} = 1.16 \text{ x } 10^{-2}$$

(2) Two threshold (Curve 2)

$$\frac{\sigma t_{min}}{t_r} = \frac{1}{5x10^{-6}} \cdot 100\sqrt{\frac{2}{3}} \times 10^{-9} = 1.64 \times 10^{-2}$$

(3) Average of seven tries of (2) (curve 3)

$$\frac{1}{5x10^{-6}} \cdot \frac{100}{\sqrt{7}}\sqrt{\frac{2}{3}} \times 10^{-9} = 6.08 \times 10^{-3}$$

SECTION IV

DATA PERFORMANCE IN A GAUSSIAN CHANNEL

4.0 General

The model FH modem will output data containing information bit errors whenever the error correcting capability of the R/S code is exceeded. Each R/S codeword corresponds to six information bits. An incorrectly decoded word will contain an average of approximately three errors. Therefore, the bit error rate will be approximately 1/2 the R/S word error rate.

The derivation of the information bit error probability is a three step process:

(a) Determine a chip error probability (See 4.1)

(b) Relate R/S word error probability to chip error probability (See 4.2)

(c) Apply correction factors to interpret data obtained from steps (a) and (b) (See 4.3)

4.1 Probability of Chip Errors in a Perfectly Timed System

In the data mode, the output of the greatest of eight circuit is sampled at the chip rate. The greatest of eight decision compares the sampled envelopes of the outputs of eight filters--one of which is a Rician variable and the other seven Rayleigh.

The chip error curve of Figure 7 is the probability that the envelope voltage from the filter containing signal is not the highest of the eight samples compared. The curve is plotted as a function of chip signal-to-noise ratio -- $A^2/2N_oW$.

4.2 Effects of R/S Coding

The R/S decoding technique in the experimental hardware is the sequential threshold decoder described in section 2.2.3(5). This

algorithm seeks a match between each seven chip received sequence and the closest R/S codeword in at least four positions. The probability of a word error, P_W, using this decoder is:

$$P_W = 1.4\ \rho_S^{\,4}\ (1-\rho_S)^3 + \left[1 - \sum_{i=4}^{7} \binom{7}{i}\ \rho_S^{\,i}\ (1-\rho_S)^{7-i}\right] \quad (17)$$

where ρ_S is the probability that a chip is correctly received as transmitted. The bracketed term is the probability of more than three errors. The first term is the joint probability that:

(a) The sequence as received contains exactly three errors.

(b) The three errors and one of the correctly received chips provide a four digit match to a valid R/S codeword (not the one transmitted).

(c) The decoder selects the wrong codeword.

The following simple derivation of the first term in equation (17) was suggested by Dr. Myron Leiter:

(1) The probability of exactly 3 errors in a received sequence (4 correctly received chips) is:

$$\binom{7}{4}\ \rho_S^{\,4}\ (1-\rho_S)^3$$

(2) The probability that the three errors and one of the correctly received digits match a codeword is

$$\frac{28}{73} = \frac{4}{49}$$

(a) There are 28 codewords that match the transmitted word in one of the correctly received chips.

(b) There are 7^3 possible values for the three chips received in error.

(3) The probability that the decoder chooses the incorrect codeword when one exists is 1/2.

(4) The joint probability of (1), (2) and (3) is:

$$1.4\ \rho_S^{\ 4}\ (1-\rho_S)^3 \text{ - the first term in equation (17).}$$

The particular form in which equation (17) has been written illustrates the difference between fine sync and data modes. In the fine sync mode it is possible to test directly for a 4 of 7 match with the transmitted codeword since the receiver has a priori knowledge of its own address. Hence, the first term of equation (17) can be set to zero.

In the data mode there is no basis for the decoder to choose between the two equally probable alternatives.

4.3 Bit Error Probability

Figure 7 plots the probability that the fine sync validation test fails -- i.e., that the receiver fails to recognize a valid address. The bit error probability in the data mode is approximately 25% of the value plotted in Figure 7.

The basis of this approximation is:

(1) The probability, P_I, of rejecting fine sync (equation (9)) is the probability that one or both of the R/S words used for address are received in error. This probability is approximately twice the word error probability.

(2) The R/S decoder delivers an output word containing six information bits. When the word is in error the average number of bit errors is approximately 3. The bit error probability is therefore approximately 1/2 P_W or 1/4 P_I. This approximation is slightly optimistic on two counts

(a) The word error probability used to compute P_I in equation (9) neglects the first term of equation (17). Approximately 4% of the sequences containing 3 errors will be incorrectly decoded in the data mode.

(b) By definition if a word is incorrectly decoded there must be at least one bit error. Since the possibility of zero bit errors in an incorrect word is excluded, the average bit error rate is slightly higher than 3.

SECTION V

PERFORMANCE IN THE PRESENCE OF CW INTERFERENCE

5.0 General

In a normal environment an FH modem may be subject to unintentional interference from a variety of unrelated signal sources conveniently modelled as CW sinusoids. In the UHF band, for example, ordinary voice transmissions are narrowband compared to the width of a single chip filter in the model FH modem. Additionally, the duration of a typical voice transmission is long compared to the 140 ms duration of a R/S word in the model FH signal structure. The most important effect of CW interference is to inhibit synchronization. This probability is discussed in section 5.1.

5.1 Sync Performance

The modem implemented in the laboratory includes a single tone interference disabling circuit. This circuit disconnects the output of any one filter containing interference from the "greatest of" circuit. The criterion used for an interference decision makes use of the fact that a valid sync pulse does not repeat the same coarse sync frequency in a seven chip sequence. The disabling process occurs after eight consecutive samples of the output of the greatest of M circuit indicate the same value. The disabled filter is reconnected for a single sample at the end of a seven chip interval. If the interference is not present in the sample, the filter remains connected until the interference criterion is again met.

Since: (1) The receiver is anticipating the arrival of the coarse sync signal from the beginning of the time slot

and: (2) The interference is assumed to be continuous,

the disabling will occur before the arrival of the coarse sync signal. Under those conditions the disabled filter will not contribute to the greatest of M decision. The detection criterion reduces to

the correct reception of at least five of the remaining six sync frequencies.

For this condition, the probability of rejecting a valid sync signal is (From equation (4))

$$P_r = 1 - \sum_{i=5}^{6} \rho_S{}^i \, (1-\rho_S)^{6-i} = 1 + 5\rho_S{}^6 - 6\rho_S{}^5$$

where ρ_S is the probability that a chip is correctly received.

Figure 5 may be used to obtain an approximate estimate of ρ_S at any given signal-to-noise ratio. This estimate is slightly pessimistic since the disabled filter will contribute no noise to the greatest of M input.

Two limitations of the single tone interference rejection concept are:

(1) The approach has no capability to cope with interference at more than one frequency.

(2) The disabling circuit may operate on a weak interfering signal when no other input is present. In this event it guarantees at least one chip error.

It is possible that the degradation of detection sensitivity under moderately low signal-to-noise ratios could be worse than the degradation suffered by not disabling the filter.

SECTION VI

SUMMARY OF RESULTS

Results of performance calculations of the model FH modem are presented in Table 3.

TABLE 3

SUMMARY OF RESULTS

PERFORMANCE CHARACTERISTIC	SYMPTOM	EFFECTS	PROBABILITY
I. SYNCHRONIZATION PERFORMANCE			
1. False Alarm	Receiver recognizes coarse sync preamble when no signal is present.	Coarse Sync Detection is tested for validity.	Subject to threshold setting-with no threshold: 9.78×10^{-4}
a.	Valid message arrives while sync decision is tested for validity.	Message is missed.	$28 \times 9.78 \times 10^{-4} = .0274$
b.	Fine sync validation test fails and receiver reverts to coarse sync mode before valid message arrives.	Receiver recovers without loss.	$1 - .0274 = .9726$
c.	Fine sync validation test finds the false alarm "valid".	Message is missed and false data outputted.	Depends on decoding algorithm used. Need not exceed: 3.8×10^{-6}

TABLE 3 (Continued)

PERFORMANCE	SYMPTOM	EFFECTS	PROBABILITY
2. Detection Failure	Receiver fails to detect valid synchronizing sequence.	Missed message.	Function of signal-to-noise ratio of receiver.
a.	3 or more errors in coarse sync seven chip sequence.	Missed message.	At 6 dB S/N 0.12
b.	Coarse sync is detected but receiver fails to decode address.	Missed message.	At 6 dB S/N (1-.12).076 = .0667
3. Timing Measurement Errors	Variance in calculated time-of-arrival due to noise and quantization.	Errors in ranging of the order of 1 ft./nanosecond.	Function of Signal-to-noise.
a.	Noise errors	"	At 6 dB S/N rms measurement error of 5.6 μ sec.
b.	Quantization error	Limits minimum variance at high S/N ratio.	At infinite S/N rms error 12.6 nanoseconds.

TABLE 3 (Continued)

	PERFORMANCE	SYMPTOM	EFFECTS	PROBABILITY
II.	DATA BIT ERROR RATE	At low S/N ratio chip error rate exceeds error correction capability of R/S code.	High error rate in decoded data.	Function of S/N ratio At 6 dB 1.9×10^{-2} At 8 dB 3.4×10^{-4}
	Single tone CW Interference	Greatest of output consistantly from same filter.	Filter output disabled. Coarse sync detection criterion changed to recognition of five of six chips.	Probability of detecting coarse sync is reduced. Roughly equivalent to requiring 1.5 dB increase in signal-to-noise ratio over value needed in Gaussian channel for given probability of sync detection.

Security Classification

DOCUMENT CONTROL DATA - R & D

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13. ABSTRACT

This report summarizes an analysis of a wide band modem in the presence of Gaussian noise or CW interference. The modem incorporates time division as the multiple access technique, multiple frequency keying as the modulation technique, frequency hopping as the spread spectrum technique and Reed Solomon coding as the error correcting technique. Particular emphasis is placed on synchronization performance using short burst signals.

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14. KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
CW INTERFERENCE						
FREQUENCY HOPPING SPREAD SPECTRUM TECHNIQUE						
GAUSSIAN NOISE						
MULTIPLE FREQUENCY KEYING MODULATION TECHNIQUE						
REED SOLOMON CODING ERROR CORRECTION TECHNIQUE						
SHORT BURST SIGNAL SYNCHRONIZATION PERFORMANCE						
TIME DIVISION MULTIPLE ACCESS						
WIDE BAND MODEM ANALYSIS						